Listing of Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

1.(Currently Amended) A method for measuring current leakage of a contact of a semiconductor device formed on or in a substrate, the method comprising the steps of:

scanning the contact with a probe ~~of a conductive atomic force microscope, the probe~~ having an electrically conductive tip;

applying a DC voltage between the substrate and the tip of the probe; and

measuring a value of a current passing through the contact to the substrate, in response to the applied DC voltage;

wherein the DC voltage applied to between the substrate and the tip of the probe during the voltage applying step is varied among at least two values, and the measuring step includes measuring the value of the tunneling current at each value of the applied DC voltage.

2.(Original) The method according to claim 1, further comprising the step of exposing the contact of the semiconductor device prior to the scanning step.

3.(Original) The method according to claim 2, wherein the contact is known to be defective.

4.(Original) The method according to claim 2, further comprising the step of attaching the substrate to a holder prior to the scanning step.

5.(Original) The method according to claim 4, further comprising the step of marking the contact prior to the attaching step.

6.(Original) The method according to claim 5, wherein the contact is known to be defective.

7.(Canceled)

8.(Currently Amended) The method according to claim [[7]] 1, further comprising the step of plotting the values of the tunneling current against the values of the applied voltage.

9.(Original) The method according to claim 1, wherein the measuring step is performed with a linear current sense amplifier.

10.(Currently Amended) A method for measuring semiconductor contact current leakage, the method comprising the steps of:

scanning a surface of a substrate having a plurality of semiconductor contacts with a probe of a conductive atomic force microscope, the probe having an electrically conductive tip;

applying a DC voltage between the substrate and the tip of the probe as the probe scans the surface of the ~~chip~~ substrate; and

measuring a value of a current passing through each of the contacts, in response to the applied DC voltage;

wherein the DC voltage applied between the substrate and the tip of the probe in the voltage applying step is varied among at least two values, and for each of the contacts, the measuring step includes measuring the value of the tunneling current at each value of the applied DC voltage.

11.(Original) The method according to claim 10, further comprising the step of exposing the contacts prior to the scanning step.

12.(Original) The method according to claim 11, wherein at least one of the contacts is known to be defective.

13.(Original) The method according to claim 11, further comprising the step of attaching the ~~chip~~ substrate to a holder prior to the scanning step.

14.(Original) The method according to claim 13, further comprising the step of marking the contacts prior to the attaching step.

15.(Original) The method according to claim 13, wherein at least one of the contacts is known to be defective and further comprising the step of marking the at least one contact known to be defective prior to the attaching step.

16.(Canceled)

17.(Currently Amended) The method according to claim [[16]] 10, further comprising the step of plotting the values of the tunneling current against the values of the applied voltage.

18.(Original) The method according to claim 17, further comprising the step of using the plot generated in the plotting step to identify one of a defective contact and a defective semiconductor structure.

19.(Original) The method according to claim 10, wherein the measuring step is performed with a linear current sense amplifier.

20.(Original) The method according to claim 8, further comprising the step of using the plot generated in the plotting step to identify one of a defective contact and a defective semiconductor structure.